

## LED Driver IC with Average-Mode Constant Current Control

### Features

- ▶ Fast average current control
- ▶ Correction for propagation delay and offset voltage
- ▶ Fixed off-time switching mode
- ▶ Linear dimming input
- ▶ PWM dimming input
- ▶ Output short circuit protection with programmable skip mode
- ▶ Input under-voltage shutdown

### Applications

- ▶ Backlighting of LCD Panels
- ▶ General Lighting

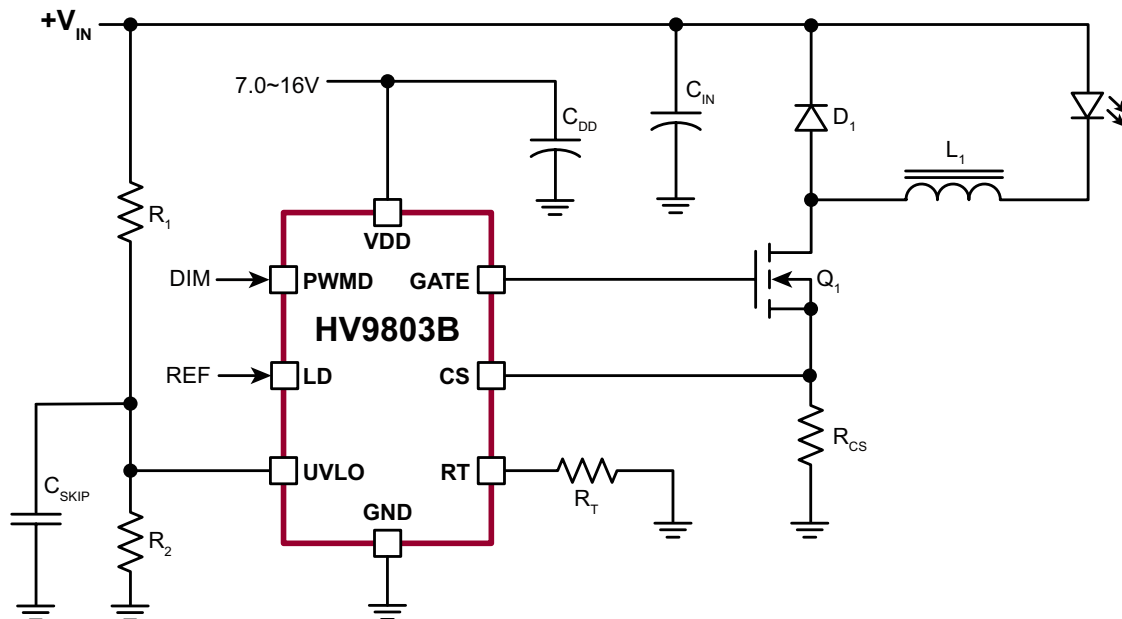
### General Description

The HV9803B is an open loop average-mode current control LED driver IC operating in a constant off-time mode. The IC features  $\pm 2\%$  current accuracy, tight line and load regulation of the LED current without any need for loop compensation or high-side current sensing. Its auto-zero circuit cancels the effect of both the input offset voltage and the propagation delay in the current sense comparator.

The HV9803B can be powered from a 7.0 to 16V supply. The IC features fast PWM dimming response. The linear dimming input LD can accept a reference voltage from 0 to 3.0V.

The IC is equipped with a current limit comparator for hiccup-mode output short circuit protection. It also features a programmable input under-voltage shutdown.

### Typical Application Circuit

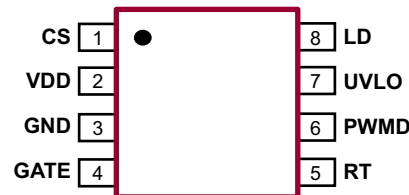


## Ordering Information

| Part Number | Package Option | Packing   |
|-------------|----------------|-----------|
| HV9803BLG-G | 8-Lead SOIC    | 2500/Reel |

-G denotes a lead (Pb)-free / RoHS compliant package

## Pin Configuration



8-Lead SOIC

## Product Marking



Y = Year Sealed  
 WW = Week Sealed  
 L = Lot Number  
 LLLL = "Green" Packaging

Package may or may not include the following marks: Si or

8-Lead SOIC

## Typical Thermal Resistance

| Package     | $\theta_{ja}$ |
|-------------|---------------|
| 8-Lead SOIC | 101°C/W       |

## Electrical Characteristics

(The \* denotes specifications which apply over the full operating ambient temperature range of  $-40^{\circ}\text{C} < T_A < 125^{\circ}\text{C}$ . Otherwise specifications are at  $T_A = 25^{\circ}\text{C}$ .  $V_{DD} = 12\text{V}$ ,  $PWMD = 5.0\text{V}$ , unless otherwise noted)

| Sym | Description | Min | Typ | Max | Units | Conditions |
|-----|-------------|-----|-----|-----|-------|------------|
|-----|-------------|-----|-----|-----|-------|------------|

### Input

|          |                               |   |   |     |     |    |                      |
|----------|-------------------------------|---|---|-----|-----|----|----------------------|
| $V_{DD}$ | Input DC supply voltage range | * | - | -   | 16  | V  | DC input voltage     |
| $I_{DD}$ | Quiescent VDD supply current  | * | - | 1.5 | 2.5 | mA | $V_{CS} = 0\text{V}$ |

### VDD Under-Voltage Lockout

|                     |   |   |      |      |      |    |                  |
|---------------------|---|---|------|------|------|----|------------------|
| $V_{DD(UV)}$        | $V_{DD}$ under-voltage lockout threshold  | * | 6.45 | 6.70 | 6.95 | V  | $V_{DD}$ rising  |
| $\Delta V_{DD(UV)}$ | $V_{DD}$ under-voltage lockout hysteresis | - | -    | 500  | -    | mV | $V_{DD}$ falling |

### PWM Dimming

|              |                                       |   |     |     |     |            |     |
|--------------|---------------------------------------|---|-----|-----|-----|------------|-----|
| $V_{EN(LO)}$ | PWMD input low voltage                | * | -   | -   | 1.0 | V          | --- |
| $V_{EN(HI)}$ | PWMD input high voltage               | * | 2.6 | -   | -   | V          | --- |
| $R_{EN}$     | Internal pull-down resistance at PWMD | - | 50  | 100 | 150 | k $\Omega$ | --- |

**Electrical Characteristics (cont.)**

(The \* denotes specifications which apply over the full operating ambient temperature range of  $-40^{\circ}\text{C} < T_A < 125^{\circ}\text{C}$ . Otherwise specifications are at  $T_A = 25^{\circ}\text{C}$ .  $V_{DD} = 12\text{V}$ ,  $PWMD = 5.0\text{V}$ , unless otherwise noted)

| Sym | Description | Min | Typ | Max | Units | Conditions |
|-----|-------------|-----|-----|-----|-------|------------|
|-----|-------------|-----|-----|-----|-------|------------|

**Current Sense Comparator**

|               |                                 |   |     |       |     |    |  |
|---------------|---------------------------------|---|-----|-------|-----|----|--|
| $V_{LD}$      | External reference voltage      | - | 0   | -     | 3.0 | V  | ---  |
| $V_{CS}$      | CS reference voltage            | * | 284 | -     | 296 | mV | $V_{LD} = 0.6\text{V}$   |
|               |                                 | * | 866 | -     | 902 |    | $V_{LD} = 1.8\text{V}$   |
| $A_{V(LD)}$   | LD to CS voltage ratio          | - | -   | 0.495 | -   | -  | ---  |
| $T_{BLANK}$   | Current sense blanking interval | * | 150 | -     | 280 | ns | ---  |
| $T_{ON(MIN)}$ | Minimum on-time                 | - | -   | -     | 760 | ns | $V_{CS} = 0.5V_{LD} + 30\text{mV}$                               |
| $D_{MAX}$     | Maximum steady-state duty cycle | * | 85  | -     | -   | %  | Reduction in output LED current may occur beyond this duty cycle |

**Short Circuit Protection**

|               |   |   |      |   |      |          |                                  |
|---------------|---|---|------|---|------|----------|----------------------------------|
| $V_{LIM}$     | Internal current reference              | - | 1.57 | - | 1.93 | V        | ---                              |
| $T_{DELAY}$   | Current limit delay CS-to-GATE          | - | -    | - | 150  | ns       | $V_{CS} = V_{LIM} + 30\text{mV}$ |
| $R_{UVLO(R)}$ | UVLO skip timer reset switch resistance | - | -    | - | 500  | $\Omega$ | ---                              |
| $V_{UVLO(R)}$ | UVLO skip timer reset voltage           | - | 200  | - | 300  | mV       | ---                              |
| $T_{ON(MIN)}$ | Minimum on-time (short circuit)         | - | -    | - | 430  | ns       | $V_{CS} = V_{LIM} + 30\text{mV}$ |

 **$T_{OFF}$  Timer**

|               |                           |   |     |     |      |               |                           |
|---------------|---------------------------|---|-----|-----|------|---------------|---------------------------|
| $T_{OFF}$     | Off time                  | - | 6.7 | 9.0 | 11.3 | $\mu\text{s}$ | $R_T = 250\text{k}\Omega$ |
|               |                           |   | 0.8 | 1.0 | 1.2  | $\mu\text{s}$ | $R_T = 25\text{k}\Omega$  |
| $I_{RT(LIM)}$ | RT over-current threshold | - | -   | 2.8 | -    | mA            | ---                       |

**GATE Driver**

|              |                       |   |       |    |    |    |                           |
|--------------|-----------------------|---|-------|----|----|----|---------------------------|
| $I_{SOURCE}$ | Gate sourcing current | - | 0.165 | -  | -  | A  | $V_{GATE} = 0\text{V}$    |
| $I_{SINK}$   | Gate sinking current  | - | 0.165 | -  | -  | A  | $V_{GATE} = V_{DD}$       |
| $t_{RISE}$   | GATE output rise time | - | -     | 30 | 50 | ns | $C_{GATE} = 500\text{pF}$ |
| $t_{FALL}$   | GATE output fall time | - | -     | 30 | 50 | ns | $C_{GATE} = 500\text{pF}$ |

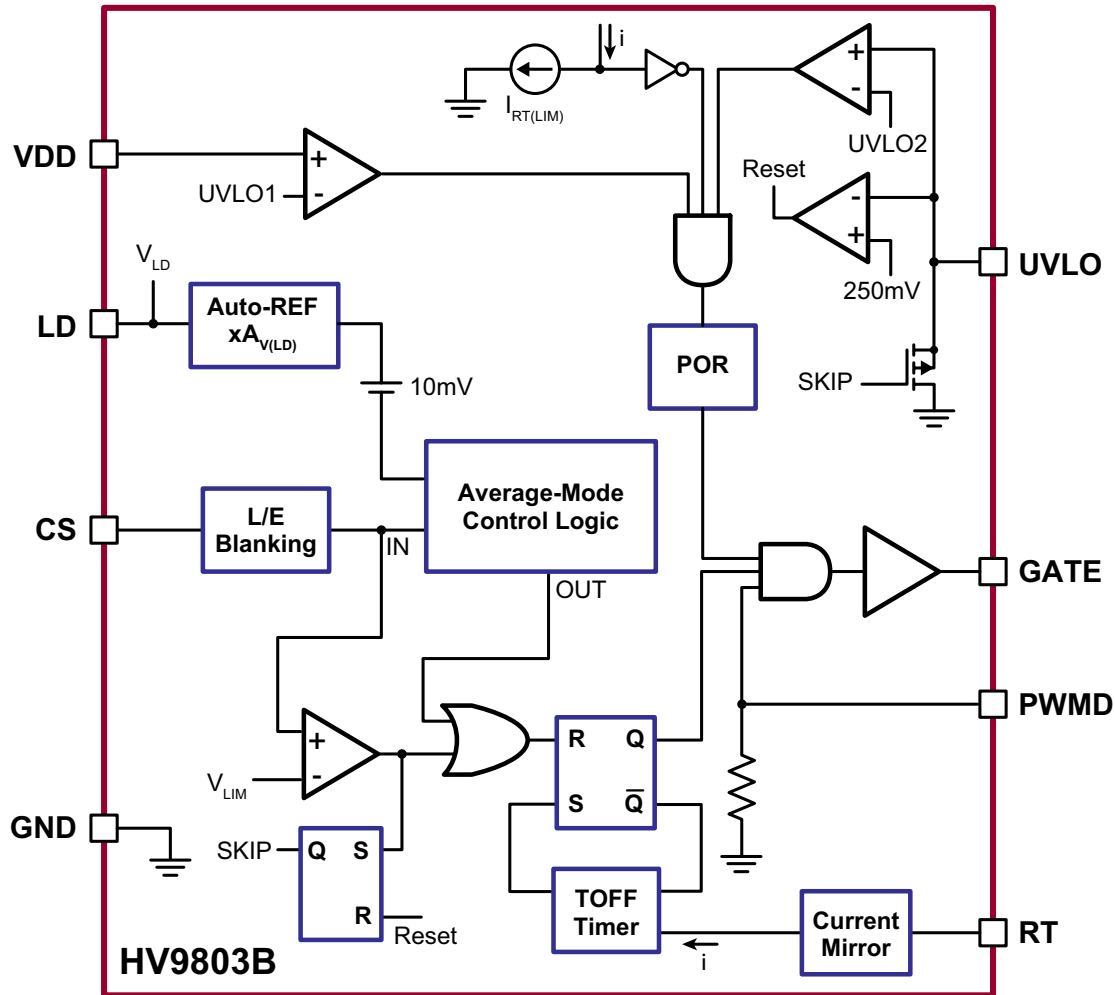
**UVLO**

|                     |  |   |      |     |      |    |                    |
|---------------------|--|---|------|-----|------|----|--------------------|
| UVLO                | Under-voltage threshold voltage            | * | 1.17 | -   | 1.29 | V  | $V_{UVLO}$ rising  |
| $\Delta\text{UVLO}$ | Under-voltage threshold voltage hysteresis | - | -    | 150 | -    | mV | $V_{UVLO}$ falling |

# Guaranteed by design

\* Limits over temperature are guaranteed by design and characterization

## Functional Block Diagram



## Functional Description

Peak-current control of a buck converter is the most economical and simple way to regulate its output current. However, it suffers accuracy and regulation problems that arise from the peak-to-average current error, contributed to by the current ripple in the output inductor and the propagation delay in the current sense comparator. The full inductor current signal is unavailable for direct sensing at the ground potential in a buck converter when the control switch is referenced to the same ground potential. While it is very simple to detect the peak current in the switch, controlling the average inductor current is usually implemented by level-translating the current sense signal from the positive input supply rail. While this is practical for relatively low input voltage, this type of average-current control may become excessively complex and expensive in the case of input voltage in excess of 100V.

The HV9803B employs Supertex' patented control scheme, achieving fast and very accurate control of average current in the buck inductor through sensing the switch current only. No compensation of the current control loop is required. The inductor current ripple amplitude does not affect this control scheme significantly, and therefore, the LED current is independent of the variation in inductance, switching frequency or output voltage. Constant off-time control of the buck converter is used for stability and to improve the LED current regulation over a wide range of input voltages. The IC features excellent PWM dimming response.

## OFF Timer

In the HV9803B, the timing resistor connected to RT determines the off-time of the gate driver, and it must be wired to GND. The equation governing the off-time of the GATE output is given by:

$$T_{OFF} = R_T \cdot 40pF$$

The  $R_T$  input is protected from short circuit. Over-current condition at  $R_T$  inhibits the IC.

## Current Sense Comparator and Timer Circuits

The function of the HV9803B's current sense comparator is similar to that of a peak current controller. However, the GATE pulse is not terminated immediately as the LD threshold is met. The GATE turn off in the  $n^{th}$  cycle is delayed by a time  $T_{2,n}$  determined by a timer circuit as follows:

$$T_{2,n} = \frac{1}{2} \cdot (T_{1,n} + T_{1,n-1})$$

where  $T_{1,n}$  and  $T_{1,n-1}$  are the times to the LD threshold in any two consequent switching cycles. This iterative control law is needed for damping sub-harmonic oscillation.

Note, that the above control law is only valid up to a maximum switching duty cycle  $D_{max} = 0.85$ . Exceeding  $D_{max}$  will cause reduction in the LED current.

Propagation delay in the current sense comparator is one of the most significant contributors to the LED current error. It must be noted that the control scheme described above does not improve this deficiency of the peak-current control scheme by itself. Moreover, it samples the propagation delay during  $T_1$  and replicates it during  $T_2$ , essentially doubling the error introduced by this delay. In order to eliminate this error, the reference voltage is corrected by an auto-zero circuit. In essence, the HV9803B samples its CS signal when the current sense comparator triggers, detects the difference between the sampled CS level and the reference input of the current sense comparator. The resulting difference is subtracted from the reference level to generate a new reference in the next switching cycle.

## GATE Output

The GATE output of the HV9803B is used to drive an external MOSFET. It is recommended that the gate charge  $Q_G$  of the external MOSFET be less than 25nC for switching frequencies  $\leq 100kHz$  and less than 15nC for switching frequencies  $> 100kHz$ .

The resulting LED current is calculated from the equation:

$$I_{LED} = \frac{0.495 \cdot V_{LD} - 7mV}{R_{CS}}$$

## Short Circuit Protection

The HV9803B is equipped with a protection comparator having a CS threshold  $V_{LIM}$ . When this second threshold is triggered, the GATE output shuts off for the duration of a restart delay, determined by the RC constant at UVLO. The capacitor  $C_{SKIP}$  is discharged below 200mV. A restart delay due to charging  $C_{SKIP}$  to the UVLO start threshold is calculated as:

$$T_{SKIP} = k \cdot R_1 \cdot C_{SKIP} \cdot \ln \left( \frac{k \cdot V_{IN} - 0.30V}{k \cdot V_{IN} - 1.17V} \right)$$

where  $k = R_2 / (R_1 + R_2)$ .

## Under-Voltage Shutdown

Under-voltage comparator input is provided to disable the IC, when the UVLO input is below a threshold. Hysteresis is provided to avoid oscillation.

## Failure Modes and Effects Analysis (FMEA)

The HV9803B is designed to withstand short circuit between its adjacent pins without damage. The following table describes the effect of such incidental short circuit conditions.

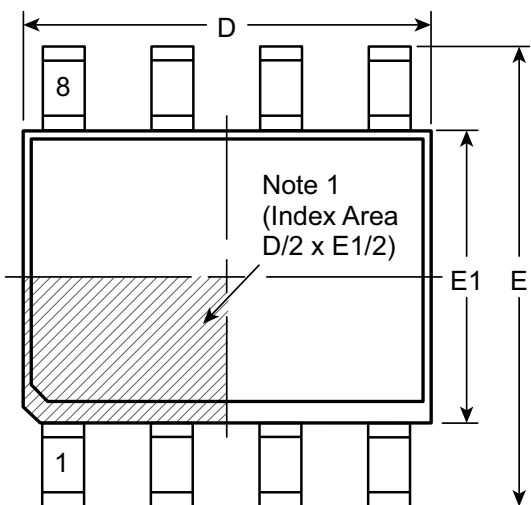
| Short Circuit Mode | Effect  |
|--------------------|---|
| CS to VDD          | The IC triggers the short circuit protection and operates in the auto-restart mode continuously.  |
| VDD to GND         | Short circuit across the 12V should cause the external bias supply over-current protection.   |
| GND to GATE        | Should cause the external bias supply over-current protection. The power MOSFET Q1 is off.  |
| RT to PWM          | <p><u>Case 1 – PWMD = Lo:</u> The RT pin sources its maximum current. GATE = 0V, and Q1 is off.</p> <p><u>Case 2 – PWMD = Hi:</u> The RT pin is pulled up, shutting off the timer. GATE is off.</p> |
| PWMD to UVLO       | This will overdrive the under-voltage threshold. However, since $V_{IN}$ UV condition is harmless to the IC, there is no effect.  |
| UVLO to LD         | LD overdrives the UVLO. If LD is lower than the UVLO threshold, the IC shuts off. No effect otherwise.  |

## Pin Description (8-Lead SOIC)

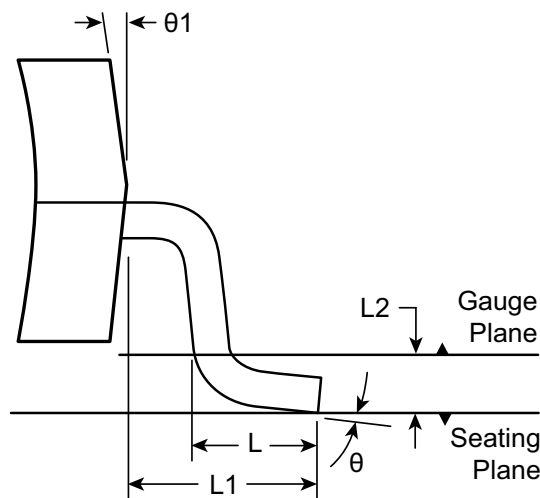
| Pin | Name | Description  |
|-----|------|--|
| 1   | CS   | This pin is the current sense pin used to detect the MOSFET source current by means of an external sense resistor.   |
| 2   | VDD  | This is the power supply input for the GATE output and input of the low-voltage regulator powering the internal logic. It must be bypassed with a low ESR capacitor to GND (at least 0.1 $\mu$ F). |
| 3   | GND  | Ground return for all internal circuitry. This pin must be electrically connected to the ground of the power train.  |
| 4   | GATE | This pin is the output gate driver for an external N-channel power MOSFET.   |
| 5   | RT   | A resistor connected between RT and GND programs the GATE off-time.  |
| 6   | PWMD | This is the PWM dimming input of the IC. When this pin is pulled to GND, the gate driver is turned off. When the pin is pulled high, the gate driver operates normally.                            |
| 7   | UVLO | This pin is the under-voltage comparator input. It is also used to form a short-circuit protection skip delay.   |
| 8   | LD   | This pin is the reference voltage input for programming the LED current.   |

# 8-Lead SOIC (Narrow Body) Package Outline (LG)

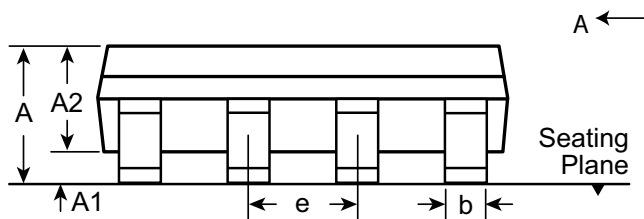
4.90x3.90mm body, 1.75mm height (max), 1.27mm pitch



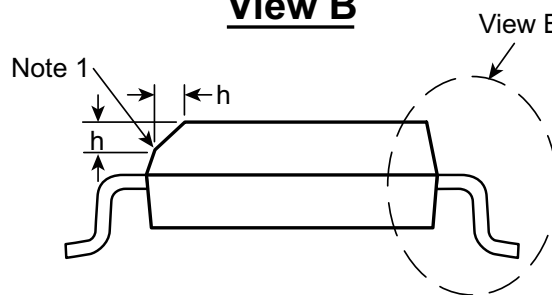
**Top View**



**View B**



**Side View**



**View A-A**

**Note:**  
 1. This chamfer feature is optional. A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.

| Symbol         | A   | A1    | A2   | b     | D    | E     | E1    | e     | h        | L    | L1   | L2       | $\theta$ | $\theta_1$ |    |
|----------------|-----|-------|------|-------|------|-------|-------|-------|----------|------|------|----------|----------|------------|----|
| Dimension (mm) | MIN | 1.35* | 0.10 | 1.25  | 0.31 | 4.80* | 5.80* | 3.80* | 1.27 BSC | 0.25 | 0.40 | 1.04 REF | 0.25 BSC | 0°         | 5° |
|                | NOM | -     | -    | -     | -    | 4.90  | 6.00  | 3.90  |          | -    | -    |          | -        | -          |    |
|                | MAX | 1.75  | 0.25 | 1.65* | 0.51 | 5.00* | 6.20* | 4.00* |          | 0.50 | 1.27 |          | 8°       | 15°        |    |

JEDEC Registration MS-012, Variation AA, Issue E, Sept. 2005.

\* This dimension is not specified in the JEDEC drawing.

Drawings are not to scale.

Supertex Doc. #: DSPD-8SOLGTG, Version I041309.

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to <http://www.supertex.com/packaging.html>.)

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